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Total Number of Pages in This Submission	30

Application Number	09/880,450
Filing Date	06/13/2001
First Named Inventor	Kenneth Barker
Art Unit	2665
Examiner Name	Steven Nguyen
Attorney Docket Number	CH9920000031US1

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Winstead Sechrest & Minick P.C.		
Signature			
Printed name	Robert A. Voigt, Jr.		
Date	11-02-05	Reg. No.	47,159

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: Barker et al.	Before the Examiner: Nguyen, Steven
Serial No.: 09/880,450	Group Art Unit: 2665
Filing Date: June 13, 2001	
Title: STM-1 TO STM-64 SDH/ SONET FRAMER WITH DATA MULTIPLEXING FROM A SERIES OF CONFIGURABLE I/O PORTS	IBM Corporation P.O. Box 12195 Dept. 9CCA, Bldg. 002-2 Research Triangle Park, NC 27709

AMENDED APPEAL BRIEF

Mail Stop Appeal Brief-Patents
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I. REAL PARTY IN INTEREST

The real party in interest is International Business Machines, Inc., which is the assignee of the entire right, title and interest in the above-identified patent application.

CERTIFICATION UNDER 37 C.F.R. §1.8

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II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellants, Appellants' legal representative or assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-28 are pending in the Application. Claims 4-6, 8, 9 (referring to claim 9 that depends from claim 8), 10-11, 15, 19, 20 (referring to claim 20 that depends from claim 19) and 21-28 are allowed. Claims 9 and 20 (referring to claim 9 that depends from claim 7 and claim 20 that depends from claim 18) are objected to as being dependent upon a rejected base claim but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 1-3, 7, 12-14 and 16-18 stand rejected. Claims 1-3, 7, 12-14 and 16-18 are appealed.

IV. STATUS OF AMENDMENTS

Appellants submitted a reply under 37 C.F.R. §1.116 filed on July 7, 2005 after the final rejection. The 1.116 reply amended claims 4, 8, 10, 15, 19 and 21 to be rewritten in independent form. The Examiner entered such amendments.

V. SUMMARY OF CLAIMED SUBJECT MATTER

In one embodiment of the present invention, a device (100) for combining at least two data signals having an input data rate into a single data stream having an output data rate being higher than the input data rate for transmission on a shared medium or vice versa, the device comprising at least two ports (102 to 108)) for receiving the at least two data signals. Specification, page 16, line 4-16; Specification, page 20, line 4-19; Figure 3, elements 100, 102, 104, 106, 108. The

device may further comprise a port scanning unit (110) for extracting data from the data signals received by the ports, characterized in that the port scanning unit (110) is configured to extract data from ports providing data streams having at least two different input data rates. Specification, page 20, lines 4-13; Specification, page 22, lines 4-9; Figure 3, element 110.

In another embodiment of the present invention, a method for combining at least two data signals having an input data rate into a single data stream having an output data rate being higher than the input data rate for transmission on a shared medium or vice versa, the method comprising the step of receiving the at least two data signals. Specification, page 16, line 4-16; Specification, page 20, line 4-19; Figure 3, elements 100, 102, 104, 106, 108. The method may further comprise extracting data from the data signals received by the ports, characterized by the step of extracting data from ports providing data streams having at least two different input data rates. Specification, page 20, lines 4-13; Specification, page 22, lines 4-9; Figure 3, element 110.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-3 and 12-14 stand rejected under 35 U.S.C. §102(e) as being anticipated by Antosik (U.S. Patent No. 6,822,975) (hereinafter "Antosik"). Claims 7 and 16-18 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Antosik in view of Goodman (U.S. Patent No. 6,636,529).

VII. ARGUMENT

A. Claims 1-3 and 12-14 are not properly rejected under 35 U.S.C. §102(e).

The Examiner has rejected claims 1-3 and 12-14 under 35 U.S.C. § 102(b) as being anticipated by Antosik. Paper No. 5, page 2. Appellants respectfully traverse these rejections for at least the reasons stated below.

For a claim to be anticipated under 35 U.S.C. §102, each and every claim limitation must be found within the cited prior art reference and arranged as required by the claim. M.P.E.P. § 2131.

1. Claims 1 and 12 are not anticipated by Antosik.

Appellants respectfully assert that Antosik does not disclose "a port scanning unit for extracting data from the data signals received by said ports, characterized in that said port scanning unit is configured to extract data from ports providing data streams having at least two different input data rates" as recited in claim 1 and similarly in claim 12. The Examiner cites element 122 in Figure 1 of Antosik as disclosing a port scanning unit and column 3, lines 2-24 of Antosik as disclosing the above-cited claim limitation. Paper No. 5, page 2. Appellants respectfully traverse and assert that Antosik instead discloses that the node (referring to element 1 in Figure 1) is configured with a multiplexer (element 122 in Figure 1) that combines up to eight different OC3/OC12-rate electrical signals into an OC48-rate electrical signal. Column 5, lines 20-24. Antosik further discloses that the mux is configured to combine two or more incoming electrical signals into an electrical signal where at least one incoming electrical signal has a first frame format at a first data rate and at least one other incoming electrical signal has a second frame format at a second data rate greater than the first data rate. Column 3, lines 2-8. Hence, Antosik discloses a multiplexer that combines two or more incoming electrical signals into an electrical signal where the incoming electrical signals may have a different data rate. However, combining two electrical signals is not the same as extracting data from the data

signals. Thus, Antosik does not disclose all of the limitations of claims 1 and 12, and thus Antosik does not anticipate claims 1 and 12. M.P.E.P. §2131.

In response to Appellants' above argument, the Examiner further cites column 1, line 64 – column 2, line 8 and column 4, lines 59-66 of Antosik as disclosing the above-cited claim limitation. Paper No. 5, page 4. Appellants respectfully traverse.

Antosik instead discloses a single circuit board for a node that is capable of packing a number of different outgoing customer signals into a single outgoing optimum-rate optical signal for transmission at a particular wavelength over an optical fiber to another node. Column 1, line 64 – column 2, line 1. Antosik further discloses that a node receives up to eight different incoming signals from its local customers, which incoming customer signals may be any combination of OC3-rate and OC12-rate signals. Column 4, lines 59-62. Antosik further discloses that the node combines (i.e., multiplexes and converts) those incoming customer signals into two copies of a single OC48 optical signal for transmission over both working and protection downstream optical fibers to another node. Column 4, lines 62-66. Hence, Antosik discloses combining different outgoing customer signals into a single outgoing signal. However, as stated above, combining electrical signals is not the same as extracting data from the data signals. Thus, Antosik does not disclose all of the limitations of claims 1 and 12, and thus Antosik does not anticipate claims 1 and 12. M.P.E.P. §2131.

2. Claims 2-3 and 13-14 are not anticipated by Antosik for at least the reasons that claims 1 and 12, respectively, are not anticipated by Antosik.

Claims 2-3 depend from claim 1, and hence are not anticipated by Antosik for at least the reasons that claim 1 is not anticipated by Antosik as discussed above in Section A(1). Claims 13-14 depend from claim 12, and hence are not anticipated by Antosik for at least the reasons that claim 12 is not anticipated by Antosik as

discussed above in Section A(1).

3. Claims 2 and 13 are not anticipated by Antosik.

Appellants respectfully assert that Antosik does not disclose "a control logic unit functionally connected to said port scanning unit for determining which of said at least two ports need to be handled within which clock cycle with regard to its input data rate" as recited in claim 2 and similarly in claim 13. The Examiner cites Figure 15 of Antosik as disclosing a control logic unit and element 122 in Figure 1 of Antosik as disclosing a port scanning unit. Paper No. 5, page 2. The Examiner further cites column 23, line 37 – column 25, line 40 of Antosik as disclosing the above-cited claim limitation. Paper No. 5, page 2. The Examiner further cites column 23, line 38 – column 25, line 55 of Antosik as disclosing the above-cited claim limitation. Paper No. 5, page 5. Appellants respectfully traverse.

Antosik instead discloses that Figure 15 discloses a block diagram of a muxing/demuxing circuit for the mux/demux board of a node. Column 23, lines 22-23. Antosik further discloses transceiver circuitry with appropriate clock-and-data-recovery (CDR) circuitry that recovers up to eight different customer signal clocks from the up to eight different OC3/OC12-rate incoming customer signals. Column 23, lines 53-57. Antosik further discloses that the customer signal clocks generated from OC3 signals have a clock rate of 155 MHZ, while customer signal clocks generated from OC12 signals have a clock rate of 622 MHZ. Column 23, lines 57-59. Hence, Antosik discloses customer signal clocks with different clock rates being generated from OC3 and OC12 signals.

Appellants respectfully note that the Examiner has not pointed out in Figure 15 which element allegedly discloses a control logic unit. Furthermore, there is no depiction in Figure 15 of element 122 which the Examiner asserts allegedly discloses a port scanning unit. Hence, Antosik does not disclose a control logic unit

functionally connected to a port scanning unit. Further, as stated above, Antosik discloses customer signal clocks with different clock rates being generated from OC3 and OC12 signals. This is not the same as determining which of the ports need to be handled within which clock cycle. Neither is the same as determining which of the ports need to be handled within which clock cycle with regard to its input data rate. Thus, Antosik does not disclose all of the limitations of claims 2 and 13, and thus Antosik does not anticipate claims 2 and 13. M.P.E.P. §2131.

4. Claims 3 and 14 are not anticipated by Antosik.

Appellants respectfully assert that Antosik does not disclose "wherein the control logic unit is configured to control said port scanning unit to access a port having a higher input data rate proportionally more often than a port having a lower input data rate" as recited in claim 3 and similarly in claim 14. The Examiner cites column 23, line 37 – column 25, line 40 as support that Antosik inherently discloses the above-cited claim limitation. Paper No. 5, page 3. Appellants respectfully traverse.

As stated above, Antosik instead discloses customer signal clocks with different clock rates being generated from OC3 and OC12 signals. The Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that generating customer signal clocks with different clock rates inherently discloses controlling a port scanning unit (Examiner asserts that element 122 of Figure 1 of Antosik allegedly discloses a port scanning unit) to access a port having a higher input data rate proportionally more often than a port having a lower input data rate. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, the Examiner must provide extrinsic evidence that must make clear that generating customer signal clocks with different clock rates inherently discloses controlling a port scanning unit to access a port having a higher input data rate

proportionally more often than a port having a lower input data rate, and that it would be so recognized by persons of ordinary skill. *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). Since the Examiner has not provided such evidence, the Examiner is merely relying upon his own subjective opinion which is insufficient to establish a *prima facie* case of anticipation. *See In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002); M.P.E.P. §2131. Thus, Antosik does not disclose all of the limitations of claims 3 and 14, and thus Antosik does not anticipate claims 3 and 14. M.P.E.P. §2131.

B. Claims 7 and 16-18 are patentable over Antosik in view of Goodman.

The Examiner has rejected claims 7 and 16-18 under 35 U.S.C. §103(a) as being unpatentable over Antosik in view of Goodman. Paper No. 5, page 3. Appellants respectfully traverse these rejections for at least the reasons stated below.

1. The Examiner has not provided any objective evidence or source of motivation for combining Antosik with Goodman.

A *prima facie* showing of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in combination, all of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art reference to make the claimed inventions. M.P.E.P. §2142. The showings must be clear and particular and supported by objective evidence. *In re Lee*, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 50 U.S.P.Q.2d. 1614, 1617 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *Id.*

The Examiner admits that Antosik does not teach have a central buffer connected to a port scanning unit into which data from all ports are written, as recited

in claim 7 and similarly in claim 18. Paper No. 3, page 3; Paper No. 5, pages 3-5. The Examiner's motivation for modifying Antosik with Goodman to have a central buffer connected to a port scanning unit into which data from all ports are written, as recited in claim 7 and similarly in claim 18, is "to prevent data loss." Paper No. 3, page 3; Paper No. 5, pages 3-5. The Examiner's motivation is insufficient to support a *prima facie* case of obviousness for at least the reasons stated below.

The Examiner has not presented a source for his motivation for modifying Antosik with Goodman to incorporate the limitations of claims 7 and 18. The Examiner simply states "to prevent data loss" as motivation for modifying Antosik with Goodman to have a central buffer connected to a port scanning unit into which data from all ports are written. The motivation to modify Antosik with Goodman must come from one of three possible sources: the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art. *In re Rouffet*, 149 F.3d 1350, 1357, 47 U.S.P.Q.2d 1453, 1457-58 (Fed. Cir. 1998). The Examiner has not provided any evidence that his motivation comes from any of these sources. Instead, the Examiner is relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 7 and 18. *Id.*

Furthermore, the Examiner's motivation does not address as to why one of ordinary skill in the art with the primary reference (Antosik) in front of him would modify Antosik by connecting to the multiplexer (element 122 of Figure 1 of Antosik which the Examiner asserts as allegedly teaching a port scanning unit) a central buffer into which data from all ports are written in light of the teachings of the secondary reference (Goodman). Antosik teaches a multiplexer in a node in an optical communication network that combines two or more incoming electrical signals into

an electrical signal where the incoming electrical signals may have a different data rate. Column 3, lines 2-8. Goodman, on the other hand, teaches that the disadvantage of a router or bridge is the complexity of processing the layer 2/3 information and the buffering of packets intended for various destinations. Column 2, lines 47-51. Goodman further teaches that the invention relates to interfaces for converting an incoming digital signal into a format for transmission on a synchronous digital network. Column 1, lines 23-25.

The Examiner has not provided any objective evidence as to why one of ordinary skill in the art would modify Antosik, which teaches a multiplexer in a node in an optical communication network that combines two or more incoming electrical signals into an electrical signal where the incoming electrical signals may have a different data rate, to connect to the multiplexer (element 122 of Figure 1 of Antosik) a central buffer into which data from all ports are written (missing limitation), in view of Goodman, which teaches converting an incoming digital signal into a format for transmission on a synchronous digital network. That is, the Examiner has not provided any connection with connecting to the multiplexer (element 122 of Figure 1 of Antosik) a central buffer into which data from all ports are written (missing limitation) with the reference Goodman, which teaches converting an incoming digital signal into a format for transmission on a synchronous digital network. Neither has the Examiner provided any connection with modifying Antosik to connect to the multiplexer (element 122 of Figure 1 of Antosik) a central buffer into which data from all ports are written (missing limitation)in order to prevent data loss (Examiner's motivation). The Examiner is merely relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 7 and 18. *Id.*

Furthermore, the Examiner admits that Antosik does not teach a step of temporarily storing data, as recited in claim 16. Paper No. 5, pages 3-5. The Examiner further admits that Antosik does not teach where the step of temporarily storing data is performed according to the FIFO concept with a speed corresponding to the input data rate of the connected port, as recited in claim 17. Paper No. 5, page 5. The Examiner's motivation for modifying Antosik with Goodman to incorporate the limitations of claims 16 and 17 is for "matching the rates between the inputs and an output signal and prevent data loss." Paper No. 5, page 6. The Examiner's motivation is insufficient to support a *prima facie* case of obviousness for at least the reasons stated below.

The Examiner has not presented a source for his motivation for modifying Antosik with Goodman to incorporate the limitations of claims 16 and 17. The Examiner simply states "matching the rates between the input and a output signal and prevent data loss" as motivation for modifying Antosik with Goodman to temporarily store data where the step of temporarily storing data is performed according to the FIFO concept with a speed corresponding to the input data rate of the connected port. The motivation to modify Antosik with Goodman must come from one of three possible sources: the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art. *In re Rouffet*, 149 F.3d 1350, 1357, 47 U.S.P.Q.2d 1453, 1457-58 (Fed. Cir. 1998). The Examiner has not provided any evidence that his motivation comes from any of these sources. Instead, the Examiner is relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 16 and 17. *Id.*

Furthermore, the Examiner's motivation does not address as to why one of ordinary skill in the art with the primary reference (Antosik) in front of him would

modify Antosik to temporarily store data where the step of temporarily storing data is performed according to the FIFO concept with a speed corresponding to the input data rate of the connected port in light of the teachings of the secondary reference (Goodman). Antosik teaches a multiplexer in a node in an optical communication network that combines two or more incoming electrical signals into an electrical signal where the incoming electrical signals may have a different data rate. Column 3, lines 2-8. Goodman, on the other hand, teaches that the disadvantage of a router or bridge is the complexity of processing the layer 2/3 information and the buffering of packets intended for various destinations. Column 2, lines 47-51. Goodman further teaches that the invention relates to interfaces for converting an incoming digital signal into a format for transmission on a synchronous digital network. Column 1, lines 23-25.

The Examiner has not provided any objective evidence as to why one of ordinary skill in the art would modify Antosik, which teaches a multiplexer in a node in an optical communication network that combines two or more incoming electrical signals into an electrical signal where the incoming electrical signals may have a different data rate, to temporarily store data where the step of temporarily storing data is performed according to the FIFO concept with a speed corresponding to the input data rate of the connected port (missing limitations), in view of Goodman, which teaches converting an incoming digital signal into a format for transmission on a synchronous digital network. That is, the Examiner has not provided any connection with temporarily storing data where the step of temporarily storing data is performed according to the FIFO concept with a speed corresponding to the input data rate of the connected port (missing limitations) with the reference Goodman, which teaches converting an incoming digital signal into a format for transmission on a synchronous digital network. Neither has the Examiner provided any connection with modifying Antosik to temporarily store data where the step of temporarily storing data is performed according to the FIFO concept with a speed corresponding to the input

data rate of the connected port (missing limitations) in order to prevent data loss (Examiner's motivation). The Examiner is merely relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 16 and 17. *Id.*

2. The Examiner has not presented a reasonable expectation of success when combining Antosik with Goodman.

The Examiner must present a reasonable expectation of success in combining Antosik with Goodman in order to establish a *prima facie* case of obviousness. M.P.E.P. §2143.02.

As stated above, Antosik teaches a multiplexer in a node in an optical communication network that combines two or more incoming electrical signals into an electrical signal where the incoming electrical signals may have a different data rate. Column 3, lines 2-8

Goodman, on the other hand, teaches a FIFO (element 490 in Figure 4) that receives inter-packet data for retiming. Column 10, lines 1-2. Goodman further teaches that the FIFO bridges the domain of the data clock based on the incoming data signal and the SDH container clock. Column 10, lines 2-4.

Based on Appellants understanding, the Examiner asserts that element 490 of Goodman teaches a central buffer. As further understood by the Appellants, the Examiner asserts that element 122 of Antosik teaches a port screening unit. The Examiner admits that Antosik does not teach a center buffer connect to the port screening unit into which data from all ports are written. Paper No. 3, page 3; Paper No. 5, page 3. The Examiner asserts that this missing limitation is found in

Goodman. Paper No. 3, page 3; Paper No. 5, page 3. By the Examiner asserting that element 490 of Goodman teaches a central buffer, the Examiner has effectively connected the FIFO (element 490) of Goodman, which resides in a linecode recognition and mapping block of a SDH framing device, to the multiplexer (element 122) of Antosik, which resides in a node in an optical communication network. Column 9, lines 48-49 of Goodman; Column 4, lines 33-36 of Antosik.

The Examiner has not presented any evidence that there would be a reasonable expectation of success in connecting the FIFO (element 490) of Goodman, which resides in a linecode recognition and mapping block of a SDH framing device, to the multiplexer (element 122) of Antosik, which resides in a node in an optical communication network. The Examiner must provide objective evidence as to how a FIFO residing in a linecode recognition and mapping block of a SDH framing device would be connected to a multiplexer residing in a node in an optical communication network. M.P.E.P. §2143.02. Since the Examiner has not provided such evidence, the Examiner has not presented a reasonable expectation of success in combining Antosik with Goodman. M.P.E.P. §2143.02. Accordingly, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 7 and 16-18. M.P.E.P. §2143.02.

3. Antosik and Goodman, taken singly or in combination, do not teach or suggest the following claim limitations.

a. Antosik and Goodman, taken singly or in combination, do not teach or suggest the limitations of claims 7 and 18.

Appellants respectfully assert that Antosik and Goodman, taken singly or in combination, do not teach or suggest "a central buffer connected to said port scanning unit into which data form all ports are written" as recited in claim 7 and similarly in claim 18. The Examiner cites column 9, line 50 – column 10, line 13 and Figure 4 of

Goodman as teaching the above-cited claim limitation. Paper No. 3, page 3; Paper No. 5, page 3. Appellants respectfully traverse and assert that Goodman instead teaches a FIFO (element 490) that bridges the domain of the data clock based on the incoming data signal and the SDH container clock. Column 10, lines 2-4. Goodman further teaches that the FIFO receives inter-packet data for retiming. Column 10, lines 1-2. As understood by the Appellants, the Examiner is asserting that FIFO (element 490) is connected to a port scanning unit for storing data from all ports. However, there is no language in Goodman that teaches that the FIFO (element 490) is connected to a port scanning unit configured to extract data from ports providing data streams having at least two different input data rates. If the Examiner is asserting that the multiplexer (element 122) in Antosik teaches the port scanning unit, then the Examiner must provide a motivation and objective evidence for connecting FIFO (element 490) in Goodman to the multiplexer (element 122) as discussed above. Furthermore, there is no language in Goodman that teaches that the FIFO (element 490) receives data from ports. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 7 and 18, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

b. Antosik and Goodman, taken singly or in combination, do not teach or suggest the limitation of claim 16.

Appellants respectfully assert that Antosik and Goodman, taken singly or in combination, do not teach or suggest "temporarily storing data" as recited in claim 16. The Examiner has not cited to any passage in either Antosik or Goodman as teaching the above-cited claim limitation. The Examiner is reminded that in order to establish a *prima facie* case of obviousness, the Examiner has the initial burden of providing a prior art reference (or references when combined) that teach or suggest all of the claim limitations. M.P.E.P. §2142. Since the Examiner has not provided such

evidence, the Examiner has not presented a *prima facie* case of obviousness in rejecting claim 16. M.P.E.P. §2142.

c. Antosik and Goodman, taken singly or in combination, do not teach or suggest the limitation of claim 17.

Appellants respectfully assert that Antosik and Goodman, taken singly or in combination, do not teach or suggest "the step of temporarily storing data is provided according to the FIFO concept with a speed corresponding to the input data rate of the connected rate" as recited in claim 17. The Examiner has not cited to any passage in either Antosik or Goodman as teaching the above-cited claim limitation. The Examiner is reminded that in order to establish a *prima facie* case of obviousness, the Examiner has the initial burden of providing a prior art reference (or references when combined) that teach or suggest all of the claim limitations. M.P.E.P. §2142. Since the Examiner has not provided such evidence, the Examiner has not presented a *prima facie* case of obviousness in rejecting claim 17. M.P.E.P. §2142.

4. Claim 7 depends from claim 2 and hence is allowable for at least the reasons that claim 2 is allowable.

Appellants note that claim 7 depends from claim 2 and hence is allowable for at least the reasons that claim 2 is allowable as discussed in Section A.

5. Claim 16 depends from claim 12 and hence claims 16-17 are allowable for at least the reasons that claim 12 is allowable.

Appellants note that claim 16 depends from claim 12 and hence claims 16-17 are allowable for at least the reasons that claim 12 is allowable as discussed in Section A.

6. Claim 18 depends from claim 13 and hence is allowable for at least the reasons that claim 13 is allowable.

Appellants note that claim 18 depends from claim 13 and hence is allowable for at least the reasons that claim 13 is allowable as discussed in Section A.

VIII. CONCLUSION

For the reasons noted above, the rejections of claims 1-3, 7, 12-14 and 16-18 are in error. Appellants respectfully request reversal of the rejections and allowance of claims 1-28.

Respectfully submitted,
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CLAIMS APPENDIX

1. A device (100) for combining at least two data signals having an input data rate into a single data stream having an output data rate being higher than the input data rate for transmission on a shared medium or vice versa, said device comprising

at least two ports (102 to 108)) for receiving said at least two data signals,

a port scanning unit (110) for extracting data from the data signals received by said ports, characterized in that said port scanning unit (110) is configured to extract data from ports providing data streams having at least two different input data rates.

2. The device according to claim 1, further comprising a control logic unit functionally connected to said port scanning unit (110) for determining which of said at least two ports need to be handled within which clock cycle with regard to its input data rate.

3. The device according to claim 2, wherein the control logic unit is configured to control said port scanning unit (10) to access a port having a higher input data rate proportionally more often than a port having a lower input data rate.

4. A device (100) for combining at least two data signals having an input data rate into a single data stream having an output data rate being higher than the input data rate for transmission on a shared medium or vice versa, said device comprising

at least two ports (102 to 108)) for receiving said at least two data signals,

a port scanning unit (110) for extracting data from the data signals received by said ports, characterized in that said port scanning unit (110) is configured to extract data from ports providing data streams having at least two different input data rates, and

at least two demultiplexing units for converting said at least two data signals into a parallel data stream of a predetermined width.

5. The device according to claim 4, further comprising at least two storage units each functionally connected to said port scanning unit (110) and one of said demultiplexing units for temporarily storing data.

6. The device according to claim 5, wherein the storage unit is formed by a FIFO and said FIFO is configured to operate with a speed corresponding to the input data rate of the connected port.

7. The device according to claim 2, further comprising a central buffer connected to said port scanning unit (110) into which data from all ports are written.

8. A device (100) for combining at least two data signals having an input data rate into a single data stream having an output data rate being higher than the input data rate for transmission on a shared medium or vice versa, said device comprising

at least two ports (102 to 108)) for receiving said at least two data signals,

a port scanning unit (110) for extracting data from the data signals received by said ports, characterized in that said port scanning unit (110) is configured to extract data from ports providing data streams having at least two different input data rates,

a control logic unit functionally connected to said port scanning unit (110) for determining which of said at least two ports need to be handled within which clock cycle with regard to its input data rate, and

a central buffer connected to said port scanning unit (110) into which data from all ports are written,

wherein the control logic unit is configured to control said port scanning unit (110) to read per access from a port having a higher input data rate proportionally more data than from a port having a lower input data rate and writing the data into said central buffer with a single clock speed.

9. The device according to claim 7 or 8, further comprising at least two demultiplexing units associated to each port, whereby the resulting data width of a demultiplexing unit is proportionally larger at a port having a higher input data rate.

10. A device (100) for combining at least two data signals having an input data rate into a single data stream having an output data rate being higher than the input data rate for transmission on a shared medium or vice versa, said device comprising

at least two ports (102 to 108)) for receiving said at least two data signals,

a port scanning unit (110) for extracting data from the data signals received by said ports, characterized in that said port scanning unit (110) is configured to extract data from ports providing data streams having at least two different input data rates,

a control logic unit functionally connected to said port scanning unit (110) for determining which of said at least two ports need to be handled within which clock cycle with regard to its input data rate, and

a central buffer connected to said port scanning unit (110) into which data from all ports are written,

wherein the control logic unit is configured to control said port scanning unit (110) to read per access from all ports the same amount of data and writing the data from a port having a higher input data rate proportionally more often into said central buffer than from a port having a lower input data rate.

11. The device according to claim 10, further comprising a byte alignment unit functionally connected to the central buffer to ensure that only frame byte aligned data are written into said central buffer.

12. A method for combining at least two data signals having an input data rate into a single data stream having an output data rate being higher than the input data rate for transmission on a shared medium or vice versa, said method comprising the steps of:

receiving said at least two data signals,

extracting data from the data signals received by said ports, characterized by the step of extracting data from ports providing data streams having at least two different input data rates.

13. The method according to claim 12, further comprising the step of determining which of said at least two ports need to be handled within which clock cycle with regard to its input data rate.

14. The method according to claim 13, further comprising the step of accessing a port having a higher input data rate proportionally more often than a port having a lower input data rate.

15. A method for combining at least two data signals having an input data rate into a single data stream having an output data rate being higher than the input data rate for transmission on a shared medium or vice versa, said method comprising the steps of:

receiving said at least two data signals,

extracting data from the data signals received by said ports, characterized by extracting data from ports providing data streams having at least two different input data rates,

converting said at least two data signals into a parallel data stream of a predetermined width.

16. The method according to claim 12, further comprising the step of temporarily storing data.

17. The method according to claim 16, wherein the step of temporarily storing data is performed according to the FIFO concept with a speed corresponding to the input data rate of the connected port.

18. The method according to claim 13, further comprising the step of writing data from all ports are written in a central buffer.

19. A method for combining at least two data signals having an input data rate into a single data stream having an output data rate being higher than the input data rate for transmission on a shared medium or vice versa, said method comprising the steps of:

receiving said at least two data signals,

extracting data from the data signals received by said ports, characterized by the step of extracting data from ports providing data streams having at least two different input data rates,

determining which of said at least two ports need to be handled within which clock cycle with regard to its input data rate,

writing data from all ports are written in a central buffer, and

reading from a port having a higher input data rate proportionally more data than from a port having a lower input data rate and writing the data into said central buffer with a single clock speed.

20. The method according to claim 18 or 19, further comprising the step of demultiplexing the incoming data stream of each port, whereby the resulting data width of a demultiplexing unit is proportionally larger at a port having a higher input data rate.

21. A method for combining at least two data signals having an input data rate into a single data stream having an output data rate being higher than the input data

rate for transmission on a shared medium or vice versa, said method comprising the steps of:

receiving said at least two data signals,

extracting data from the data signals received by said ports, characterized by the step of extracting data from ports providing data streams having at least two different input data rates,

determining which of said at least two ports need to be handled within which clock cycle with regard to its input data rate,

writing data from all ports are written in a central buffer, and

reading per access from all ports the same amount of data and writing the data from a port having a higher input data rate proportionally more often into said central buffer than from a port having a lower input data rate.

22. The method according to claim 21, further comprising the step of performing a byte alignment to ensure that only frame byte aligned data are written into said central buffer.

23. A method comprising the acts of:

(a) receiving, in ports of a network device, frames in which at least two data traffic with different transmission rates are encoded;

(b) reading frames from the ports into a receiving path with a port scanning unit;

(c) examining the frames with a plurality of processing units operatively disposed within the receive path;

(d) as each processing unit, in the plurality of processing units, examines the frames extracting data encoded in particular section of said frame and forwarding remaining portion of the frame to downstream processing units;

(e) repeating step (d) by downstream processing units until the payload section of the frame remains;

(f) receiving the payload section of the frame in a payload handling unit which parses the content into specific data types based upon the encoded data.

24. The method of claim 23 further including the act of receiving the specific data type in a Utopia level 4 interface which transmits the specific data type to a link layer device or DS.sub.3 mapper device.

25. The method of claim 23 wherein the extracted data is stored in memory units.

26. A device comprising:

a data scanning unit that accesses ports of a network device to read data frames in which a payload of at least two data traffic at different rates are encoded;

a plurality of storage elements that store information extracted from the data frames;

a plurality of Receive processing units operatively coupled in series, wherein each one of the plurality of processing units is coupled to selected ones of the storage elements and said each one of the plurality of processing units examining the frame and extracting information from predetermined portion of said frame and forwarding the remaining portion of said frame to downstream processing units; and

a payload handler receiving the payload in said frame and parsing the payload to generate different data types embedded in said payload.

27. The device of claim 26 further including a plurality of transmit processing units operatively coupled in series and cooperating to generate and transmit to said ports a frame containing a payload of at least two data traffic at different rates.

28. The device of claim 27 further including a plurality of memories selectively coupled to selected ones of the plurality of transmit processing units.

EVIDENCE APPENDIX

No evidence was submitted pursuant to §§1.130, 1.131, or 1.132 of 37 C.F.R. or of any other evidence entered by the Examiner and relied upon by Appellants in the Appeal.

RELATED PROCEEDINGS APPENDIX

There are no related proceedings to the current proceeding.